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SUBJECT: OPERATION OF MAGNETIC DRUMS WITH WWI

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From: E. S. Rich

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Abstract: Two magnetic drum systems are being constructed by Engineering Research Associates of St. Paul for use with the Whirlwind Computer. One of these, the auxiliary storage drum, will be used for a large capacity storage to supplement electrostatic storage. The second system, the buffer drum, will be used to assemble asynchronous input data from multiple inputs so that it can be later transferred to the computer when called for. Communication between these drums and the computer will be by way of the in-out register. Use of in-out control will be required and in this sense the drums will function as units of terminal equipment. Although other methods for integrating the systems have been considered, the method proposed was chosen because of its relative simplicity. Two additional in-out orders are proposed to provide for block transfers between the drums and the computer making a total of five orders being involved in operation of units of terminal equipment. The modes of operation of the auxiliary drum are worked out in a fairly complete manner but many of the details of buffer drum operation still remain to be specified. Some flexibility in the design and construction of the buffer drum is being planned to allow for integration of new types of inputs and outputs which may be desirable in the future.

1.0 DESCRIPTION OF THE TWO DRUM SYSTEMS BEING BUILT BY E.R.A.

At the present time Engineering Research Associates of St. Paul is constructing two magnetic drum systems for use with the Whirlwind Computer. These have been designated as the auxiliary-storage-drum system and the buffer-drum system. The logical designs of these two systems have certain significant differences. A general description of these designs follows.

1.1 Auxiliary Storage Drum.

The auxiliary-storage-drum system (auxiliary drum) is similar to a standard drum system such as E.R.A. used in their 1101 computer. A simplified block diagram of the auxiliary drum system is shown in the attached drawing SA-50699. It has a total of 194 magnetic heads which are divided for our purposes into groups of 16 heads each. There are therefore 12 16-digit groups provided on this drum with the remaining two heads used for timing and bracket tracks. Ten additional heads could be added later if desired. The drum is designed so that 2048 pulses can be recorded in any one track around the circumference of the drum, giving a total storage capacity of 2048 x 12, or 24,576 16-digit registers. In selecting a drum register, angular position of the drum is determined by the angular position counter (APK) which counts the pulses on a timing channel, starting with a reference position determined by a pulse recorded in a bracket channel. The selection of a particular register in a given group is done by comparing the contents of this counter with the desired address read into 11 digits of the storage address register (SAR). Selection of a particular group out of the 12 groups is done by a crystal matrix switch controlled by 4 flip flops in the storage address register. The complete selection of a particular register on the drum, then, is accomplished by inserting a 15-digit word into a storage address register, 11 digits of which are compared against the contents of the angular position counter and 4 digits of which accomplish selection of the desired group.

The auxiliary drum is provided with one set of 16 reading amplifiers and one set of 16 writing amplifiers. The connection of the reading amplifiers to the desired set of 16 heads is accomplished by low-level crystal gating at the inputs of the amplifiers. The connection of the writing amplifiers to the desired set of heads is accomplished by relay switching. The writing amplifiers are of the hard tube type so that, within a given field, writing can be accomplished at each successive angular position. However, there is a duty factor limitation on this writing imposed by heating within the heads which limits the average speed of recording to every other drum position. In switching the reading amplifiers from one group to another a wait period of at least 30 microseconds is necessary in order for transients in the reading amplifiers to die out. In switching the writing amplifiers from one group to another a period of 24 milliseconds is required to allow for operation of the relays which accomplish the writing-group selection.

1.2 Buffer Drum.

The buffer drum contains 162 single heads divided into 10 16-digit groups, and in addition has 12 dual heads which serve a special function to be described later. A block diagram of the buffer drum is not included because interconnection of all the components in the system will not be done by the manufacturer. This is to allow efficient integration of new inputs which may be needed at a later date. On this drum separate writing amplifiers are provided for each of the heads in order to eliminate the relay switching which is used in the auxiliary drum. Selection of a particular group of heads for writing is accomplished by electronic switching and therefore can be done without delay. At least 2 and possibly 4 sets of reading amplifiers will be provided since a single set of amplifiers cannot be switched between two or more groups where reading from one of these groups to the computer is to take place simultaneously with writing onto another group from some external source. A combination of drum groups which does not experience simultaneous reading and writing can be connected to a single set of reading amplifiers and in such cases selection of the desired group will be accomplished by low-level gating at the input to the amplifiers as was done in the auxiliary drum.

The buffer drum will be provided with an angular position counter to indicate the present angular position and with a storage address register which can select a particular drum register. However, the counter and the coincidence detector used in this system will be designed for greater flexibility than is the case with the auxiliary drum. The angular position counter will have outputs capable of driving a crystal matrix so that a pulse distributor can be built to provide timing pulses that do not occur on every angular position. With this feature some interleaving of data on the drum can be accomplished.

There are some further differences in the buffer drum relating to the manner in which writing groups are selected and in which register positions for writing and reading are selected. The latter selection involves the use of dual heads in a special way which will be described later.

2.0 PROPOSED USES

2.1 Auxiliary Storage Drum.

The auxiliary storage drum will be used primarily for storage of numerical data and computer subprograms, and hence transfers of information will take place only between the drum and electrostatic storage. These transfers will take place by way of the in-out register and in this sense the drum operates as a piece of terminal equipment. The transfers can be either single word or blocks of words. The block transfers will take place at nearly the maximum speed which can be achieved by ES and therefore are high speed transfers. Utilization of the drum in this manner will make it possible to store programs or other large sections of information for easy access by the computer. It does not appear practical to arrange for this drum to communicate with other pieces of terminal equipment independently of computer control because of the large amount of special control equipment that would be necessary.

2.2 The Buffer Drum.

The buffer drum is to be used for temporary storage of data which is being communicated between the computer and certain special types of terminal equipment. Principally it is to be utilized where input data is arriving in a random and asynchronous manner from more than one source. In order to handle data of this type without the use of some such buffer storage it would be necessary for the computer to be ready at all times to receive data and store it in ES. The buffer drum accumulates data of this sort so that it is only necessary for the computer to remove the information from the drum at relatively infrequent intervals and at points in the computer program when it is convenient to do so.

Use of the special dual heads makes it possible to determine whether or not the data which has been placed in a drum register by an external input has been read to the computer. In this they provide the facility for locating "empty" registers for recording from the external source and for locating "filled" registers when reading to the computer. The distinction between "empty" and "filled" registers is obtained by binary digits recorded on "status tracks" by the dual heads. Such a facility is necessary since both the reading and the recording are not under the control of the computer.

The buffer drum may also be used for receiving information at a slow rate from inputs such as typewriters or teletype lines and later transferring this information to the computer at a high rate by means of a block transfer. Conversely it could handle output information where the computer would perform the recording at its maximum speed; the information would then be read to an output device such as a typewriter at the necessary slow speeds.

3.0 OPERATION OF THE AUXILIARY DRUM WITH WWI

3.1 Considerations Affecting Choice of Method of Control.

There are several factors which influence the selection of the control system which might be used with the auxiliary drum. The more important considerations are the following:

1. Cost in equipment to be constructed.

2. Efficiency in use of computer time.

3. Simplicity from the programmer's viewpoint.

4. Flexibility in modes of operation.

Some of the above are in conflict so the "best" design must be a compromise. Discussions of these points are given in the following paragraphs. It is obvious that the simplest control is most desirable from the standpoint of the engineering required to design, to install, to debug, and to maintain the equipment.

The most efficient use of computer time occurs if the transfers between the drum and electrostatic storage are carried out simultaneously with useful calculations. To achieve this type of operation would require two independent banks of ES and therefore is not feasible in WWI. A less efficient but more practical arrangement for WWI results when the computer program is held up only long enough for the transfers required, and is not held up during searching. For single word transfers the latter facility is already available in in-out control. However, for block transfers, if the drum is connected as a piece of terminal equipment with the present in-out control, it would be necessary for the computer to wait after ordering a transfer until the beginning of the block of information is located on the drum. On the average, then, there would be an 8-millisecond wait at the beginning of each block transfer. To eliminate this wait, a control would be necessary which would allow the drum to break into the computer program at the time the desired storage location on the drum is reached. This procedure would require an expansion of our present in-out control and a different type of in-out interlock.

Since the purpose of the in-out switch is to permit a programmer to select many different pieces of terminal equipment, some of which have several different modes of operation, it is evident that the inclusion of the in-out switch and the associated terminal equipment will make it more difficult for the programmer to learn to use the order code fluently. In a sense, the addition of the in-out switch means an extension of the control matrix from the present 32 orders to two or three times this number. This can easily place a large burden on the programmer, particularly if care is not taken to select the modes of operation in such a manner that they can be defined easily in the instructions for the code.

The large number of possible positions of the in-out switch creates a tendency for one to arrange many different modes of operation for units of terminal equipment. In the case of magnetic drums, if other considerations did not prevail, it would be desirable to permit communication from the drum not only to the computer but also to other units such as punched tape, magnetic tape, and display scopes.

3.2 Possible Alternatives.

There are two principal methods in which operation of the auxiliary drum with the computer might be obtained. First, the drum might be connected as a piece of terminal equipment in which transfers between the drum and the computer would be controlled by orders similar to those used for other types of terminal equipment. Second, a control might be designed which would allow the drum to break into the computer program just before the desired starting location on the drum reaches the heads.

Each of these two alternatives has its own advantages and disadvantages. The advantages of the first method are its simplicity and the ease with which the drum can be integrated with in-out control, while its disadvantages are that some computer time is lost and that manipulation of the necessary control orders is somewhat burdensome for the programmer. The second method eliminates most of the time lost by the computer but requires a substantial amount of new circuit construction and possibly some changes in the presently planned control of external units. Although the orders which command transfers in this method might be simpler for the programmer to use, an additional complication is introduced in determining whether a requested block transfer has been carried out. In order to determine whether the transfer has been completed, so that the computer will not refer prematurely to an ES register whose contents are to be changed as a result of the transfer process, it is necessary either to provide a special check order, which increases programming worries, or to provide a complicated interlock which will stop the computer if an attempt is made to refer to an ES register which is involved in the block transfer.

There are several minor considerations in the choice of a control method which have been studied and in which alternatives exist. Principally, these involve the detailed functioning of the control orders which might be used. For example, in using the drum the following modes of operation might be desirable:

1. Read a block of information starting at the drum address already held by the drum address register.

2. Read a block of information from the drum starting at some new drum address.

3. Read a block of information from a new drum address in a new group. This differs from the mode above in that it is necessary to switch the drum reading amplifiers from one group of heads to another.

4. Read a single word from the drum from the address already in the drum address register.

5. Read a single word from a new drum address.

6. Read a single word from a new drum address and a new group.

7. Six additional modes similar to those above except recording operations rather than reading operations would be carried out.

Various ways of providing the above modes of operation have been considered. The possibilities are to use different settings of the in-out switch to specify the modes completely, or to use switch settings in conjunction with various reading and recording orders to identify the type of operation desired. The choice in this matter appears to depend both on the amount of equipment which is needed to provide all the necessary control signals in their proper time sequence as well as on the complications added to programming. For example, to use the setting of the switch to define whether there is to be a reading or a recording operation, and also whether it is to be a block transfer or a single word transfer, would reduce the number of orders in a program but would require that the number of CPO units on the control matrix presently involved in in-out operations be approximately doubled.

3.3 Proposed Installation.

For the initial installation of the auxiliary drum it is proposed to use the first of the two alternatives described in section 3.2 in which the drum is connected to the present in-out system as another unit of terminal equipment. This permits the most straightforward design and appears to be the only one which we can reasonably expect to engineer within the period from now until the drums are to be delivered. Its principal disadvantage of causing lost computer time is less objectionable as the capacity of ES storage is increased.

3.31 Modes of Operation.

The following modes of operation to be selected by the in-out switch are contemplated for the initial installation.

1. Read from the drum register and group which is already selected by the drum storage address register (SAR). The SAR is connected so that it indexes to the next register after each transfer, so, if a new drum address is not specified prior to a transfer, the word will be taken from the register following that last referred to. The distinction as to whether a single word or a block is to be transferred is made by separate orders following the switch selection order.

2. Read from a new drum register in the same group. This mode is identical to the one above except a new angular position on the drum is selected.

3. Read from a new drum register in a new group. This is identical to the above modes except both a new group of heads and a new angular position are selected.

Three additional modes would also be provided to permit recording on the drum. These would be similar to the above modes except a recording rather than a reading function would be carried out.

3.32 Orders Needed.

A total of five in-out orders will be required to control the drum operation. Of these the si, rc, and rd orders are essentially the same as those presently planned for the new in-out system. Two additional orders to specify the block transfers are needed. Tentatively, these are called bi (block input), and bo (block output). The principal functions of these orders will be described in the following paragraphs with reference to the modes of operation outlined in section 3.31 above.

3.321 si. The si order causes the in-out switch to be set to the position designated by the address section of this order. In addition to selecting the drum, the switch setting specifies certain control functions that are unique to the mode of operation called for. Consequently, an si order with a different address section is needed for each of the 6 modes of operation listed in 3.31. In two of these modes an 11-digit word must be read into the drum storage address register to specify a new angular position on the drum, and in two other modes a 15-digit word must be supplied to the drum to designate both angular position and group. These words are supplied by a transfer from the accumulator during the si order. If the si order used is one calling for a new drum address, it is evident that the programmer must provide the proper information in AC before the si order is performed.

3.322 rd. The rd order used following an si order specifies that a single word rather than a block is to be transferred from the drum to the computer. It can be used following only those si orders whose address sections refer to reading operations. A detailed analysis of the effects of improper sequencing of the in-out orders will be made the subject of a separate memo, but in general incorrect use of these orders will result in either an in-out alarm or an inactivity alarm. The address section of the rc order as presently proposed specifies into which ES register the word will be put.

Some alternative designs for the single-word-transfer orders (rd and rc) have been suggested. These provide certain features which may be of value to programmers and therefore are being considered. It should be noted that changes in these orders will apply to all external units and not only to drums. The principal suggestions are the following: (1) Instead of transferring words between IOR and ES, the orders might transfer between IOR and AC since, in many cases, single words will be processed by the computer in the interval of time between transfers. Adoption of this arrangement would require a change in the method proposed for supplying data to the display decoders. (2) If transfers were between IOR and AC, the address section of the single-word-transfer orders might be used for shifting the contents of AC. At present there seems to be little advantage to such a feature. (3) Instead of (2) the address section might be used as a subprogram address if a memory element were provided in ICC to indicate whether or not an in-out process had been completed, and if the rc and rd orders were made to function like cp orders. Essentially, this arrangement would serve the function of the present in-out interlock by preventing a program from proceeding beyond a certain point until an in-out operation had been completed. In addition, it would make it possible for a programmer to utilize computer time between in-out operations without detailed calculations of the actual time duration of his programs. (4) No study has been made of the amount of equipment needed to accomplish the type of operation described in (3) but if the equipment is excessive the same result might be obtained more simply by the use of a special check order in conjunction with the in-out orders.

3.323 bi. The bi order following an si order calls for the transfer of a block of information from consecutive registers on the drum into consecutive registers in ES. This order is assigned with no program timing similar to the present ri order, and in fact will replace the ri order. Since, in a block transfer, it is necessary to specify not only the starting address on the drum and starting address for ES, but also the number of words which are to be transferred, some means must be provided for stopping the transfer process when the desired number of words have been read. To do this the in-out delay counter will be used to count the words which have been transferred. To specify the number of words in a block the programmer must insert this number into the accumulator before the bi order is performed. During the bi order the contents of AC are read to the IO delay counter so that it will produce an end-carry after the desired number of words has been read in. As in the case of the rd order, the bi order can be used only following those si orders which involve reading operations.

There is one important difference between the proposed bi order and the present ri order which is of interest to programmers. This difference is in the way in which the computer returns to the proper point in its program following the block transfer. In the ri order, as originally planned, the storage switch is indexed to select successive ES registers for the incoming words by counting in the program counter. Therefore, at the end of the transfer, the contents of the program counter have to be restored to the value that will set up the storage switch to extract the next desired order from ES. In the bi order the contents of the program counter will be unchanged during the block transfer process. To accomplish the necessary selection of successive ES registers for the words being read in, the storage switch will be indexed in the following manner. During the bi order the right-11 digits of the program register will be inserted into AC, one will be added to this number in AC, and the result will be read back to the program register for each of the words occurring in the block transfer. When the IO delay counter end-carry occurs, which signifies the end of the block transfer, the control matrix will be switched to program timing on the proper time pulse, one will be added to the contents of the program counter, and the next order will be automatically extracted from storage. At the end of the bi order, then, the A-register will hold the address of the last ES register read into and the accumulator will hold the same number plus one. This information is of no particular value in the case of block transfers from the auxiliary drum where the block length is known, but it can be utilized in one mode of reading from the buffer drum. If one wishes to read the information from all the "filled" registers in one section of the buffer drum, the IO delay counter can be used to determine when the desired section has been scanned and the contents of the accumulator then would show how many filled registers were found.

3.324 rs. The rs order takes a single word from the ES register specified by the address section of this order and places it in the in-out register so that it may be recorded on the drum.

The drum address where this word will be placed is provided by the si order as has been described in section 3.321. An si order specifying a recording operation must precede these rc orders.

3.325 bo. The bo order following an si order calls for a block of information to be recorded on the drum. This order must be handled in a manner similar to the bi order. That is, a number must be placed in the accumulator before this order occurs so that the in-out delay counter will be set up to count the number of words in the block. The address section of the bo order specifies the starting ES register, while the number transferred from the accumulator to the drum storage address register during the si order specifies the starting drum address. The bo order also has no program timing and indexing of the storage switch is accomplished by transfers between PR and AC with counting done in AC.

3.33 Typical Order Sequences.

To illustrate the use of the orders described above some typical sequences of orders will be given.

3.331 Reading a Single Word from the Drum. If the mode of operation desired is to read the word from the drum register which is already contained in the drum storage address register, no transfer from the accumulator to the storage address register takes place on the si order and the sequence required for each word read is si, rd. If the mode of operation desired is one in which a new drum register is to be specified, the si order in the above sequence must be preceded by a ca order to insert the proper drum address in the accumulator. The si order initiates the reading operation and, as soon as the proper drum address is located, a single word is transferred to the in-out register. The rd order can then take this word and transfer it to the ES register specified by the address section of this order. To read several words from the drum it is necessary to program a separate si for each transfer. Since the drum storage address register indexes to the next position after each read operation, one can get words from the consecutive drum addresses without the necessity for specifying each address with a word placed in the accumulator. However, these consecutive words would come approximately 16 milliseconds apart since it would require a drum revolution to locate each new address. The wait period comes between the si and the rd orders so that computer time is not lost provided at least 16 milliseconds of program is interspersed between these two orders.

3.332 Recording Single Words. The sequence of orders for recording single words is si, rc. As in the case of reading, the si must be preceded by a ca order if the drum address desired is not the one presently held by the drum storage address register. In the case of recording, however, words may be placed in successive drum registers without repeating the si order for each transfer. A recording operation is initiated by the rc order whereas a reading operation is initiated by the si rather than the rd order. In recording a sequence of single words at successive drum addresses, at least a 16-millisecond interval must occur between successive rc orders. In this case the wait period follows the rc order rather than the si order.

The differences in handling the orders for single-word reading and for single-word recording are a source of confusion to a programmer. Although it is possible to design a control so that the need for repeated si orders during reading is eliminated, the arguments thus far presented for this do not seem to warrant the increased complexity in the control that would result if the change were made.

3.333 Reading a Block from the Drum. If it is desired to read N words from the drum starting at drum register L and to place these words into ES registers starting at register E, the following sequence of orders would be necessary:

ca RC(L)

si ---

ca RC(N)

bi E

The first order in this sequence transfers the drum starting address L into the accumulator. On the following si order this address is transferred to the drum storage address register and the reading mode of operation is selected. On the third order the number of words contained in the block is inserted into the accumulator and on the last order this number is moved to the in-out delay counter and the block reading operation is initiated. The computer must be stopped at this point since the desired drum starting address may come up immediately. However, it is equally possible that this starting address has just been passed so that a 16-millisecond wait is necessary. Therefore, on the average it will require 8 milliseconds to locate the desired starting address while accomplishing block transfers from the drum. Once the drum starting address is located, the transfers of successive words take place at 64-microsecond intervals. This time interval is obtained by arranging the address location circuits of the drum so that successive adresses refer to drum positions which are physically 8 registers apart. This interval was chosen as being the most convenient value to obtain which would allow ES to operate at approximately its maximum speed. Since the bi order contains no program timing pulses, no further orders in the program are executed until the block transfer is over. After each word is transferred both the program register and the drum storage address register are indexed to handle the next transfer. When the desired number of words have been read in, an end-carry pulse from the in-out delay counter operates to terminate the bi order and switches the control matrix back to program timing so that the next order in the program will be executed.

3.334 Recording a Block on the Drum. The sequence of orders for recording a block of information on the drum is the same as for reading a block except the si order used must have an address which specifies a recording mode of operation, and the bo order is used in place of the bi order. As in the case of the block-reading operation the computer must be stopped on the bo order to allow for the possibility that the starting drum address will be located immediately.

4.0 OPERATION OF THE BUFFER DRUM WITH WWI.

The details of how the buffer drum will be integrated with the computer have not been completely developed as yet. However, certain functions which must be accomplished are clear so that some observations on the use of this drum are possible. Because it is provided with a small number of dual heads many more possibilities exist for connecting this drum with various pieces of terminal equipment and with the computer. Only a few of the most likely types of connection will be described in this memo.

4.1 Asynchronous Data from Multiple Inputs.

Since the main purpose of the buffer drum is to act as temporary storage for data which may arrive at the computer in a random fashion from a number of sources, a consideration of the use of the buffer drum for this purpose will be discussed first. Two broad classifications of this asynchronous type of data can be made. First, that which arrives from a given input at a rate higher than one piece per drum revolution, and second, that which comes at intervals greater than the drum rotation period. For the purposes of this memorandum these are referred to as high-data-rate inputs and low-data-rate inputs, respectively.

4.11 High-Data-Rate Inputs.

When information is arriving more often than once each drum revolution, it is impossible to record this information at a specific drum location. To handle data of this type it is planned to make use of the dual heads to determine whether or not a given drum register contains information which is later to be read to the computer. Each piece of new data will be recorded in the first empty register which is located and the process allowed to continue until a reasonable number of registers have been filled or until the computer is able to extract this information from the drum for use inside the computer. By providing two drum storage groups such that the inputs are alternately switched from one group to another, it is possible for the computer to have access to recorded information without interrupting the recording process. If an arrangement is made to switch the recording from one field to another sufficiently often, then the probability that there will always be an empty register in which to put each incoming piece of information will be high.

The problem of handling multiple inputs having data of this sort will be taken care of by interleaving information from the various inputs in the drum registers of a given group. For example, with eight inputs, every 8th register in a group will be assigned to the same input. (Data from a given input must be put at least 8 drum registers apart to allow time for operation of ES during block reading.) The number of inputs which can be interleaved in one drum group is determined by the minimum time interval between successive pieces of data on a given input line and the rate at which the inputs are switched to another field so that the computer can extract information from the first field; i.e., the number of drum positions which pass under the recording heads during the interval between pieces of data, and the total number of pieces of input data that arrive between reading operations to the computer determine the probability of finding an empty register for the information.

If the number of inputs that must be handled exceeds the number which can be interleaved in one group, then these inputs can be divided among two or more groups for simultaneous recording. For each such division of inputs, actually two drum groups are required in order to permit the computer to extract information without interrupting the recording process.

It will be noticed that most of the recording functions for the system described above (i.e., selection of register for recording, transfer of information to the drum, and interleaving of multiple inputs) are accomplished independently of computer control. The computer, however, does govern the reading processes in a manner similar to that used with the auxiliary drum. One principal mode of operation appears to be required: i.e., read all new information that has arrived from a given input. This will be a block transfer in which the dual heads function to locate registers containing new information and in which the address supplied by the computer governs which group is selected and which of the interlaced registers in a group will be scanned. Other than to specify which input is involved, the starting drum address is immaterial, and the block transfer is terminated after the drum has made one complete revolution. This point is determined by counting drum timing pulses in the IO delay counter.

Other reading modes which may be useful are (1) reading a given number of words, or (2) starting at a given address, reading consecutive registers until an empty one is found. The latter mode applies to low-data-rate inputs described below.

4.12 Low-Data-Rate Inputs.

Information which arrives at the computer at a rate less than the frequency of drum revolutions can be handled so that each piece of information is put on a predetermined location on the drum. Since it is desired that recording of this input data will not involve computer control in any way, the use of the standard drum address system (SAR) for locating the desired recording position is prohibited. However, the dual heads can be used effectively to arrange successive pieces of input information in consecutive drum registers. This would be done by building a control which would require that a recording take place in the first empty register following a filled one, or, in the case of the first piece of information to arrive, following some reference position. Examples of data that could be handled this way are those from typewriters, teletype lines, or photoelectric readers.

As in the case of the inputs discussed in the preceding section, more than one low-data-rate input can be handled by interleaving their information in the registers within a single group. In order for the computer to collect the data corresponding to a given input, it is necessary only to call for a block read-in of the data found in the drum registers corresponding to that input.

4.2 Buffer Storage for Outputs.

A dual-head control channel appears to be useful to permit operation of low-data-rate outputs such as typewriters or teletype sending equipment from data recorded on a drum. These heads would function to select the first filled register following an empty one and in this manner cause successive words to be read from consecutive drum registers. The output data would be recorded on the drum by a block transfer from ES so the above scheme constitutes an excellent speed-changing mechanism for matching the slow speeds of typewriters and teletype equipment to the high speeds of ES.

4.3 Other Uses of the Buffer Drum.

4.31 Storage for Display.

Some consideration has been given to the use of one or more groups on the buffer drum for storage of data to be displayed on a scope. This application is suggested by the fact that the periodic reappearance of a given piece of data under the reading heads on the drum would satisfy the requirement for repeated intensification of an elementary spot in a scope display. In this manner a persistent display pattern could be obtained without having to recalculate all the spots periodically or to rely on cathode ray tubes with long persistence phosphors.

Several problems appear to be involved in the design of such a display system and at present they seem to outweigh the advantages that might be gained. Some of the disadvantages are:

(1) Only a relatively small amount of data could be recorded in one group if a complete display were to be obtained each drum revolution. Two words would have to be recorded for each spot and pairs of words would have to be spaced apart to give time for ES operation during recording and for scope intensification.

(2) Increasing the storage capacity to improve (1) would mean considerable additional equipment. If two groups were used to record the two elements of display data, an additional set of drum reading circuits would be necessary. If data were interlaced and more than one drum revolution used to give a complete display, the control circuits would be somewhat more complicated.

(3) An additional set of deflection decoders would be required to operate the display system.

4.32 Additional Auxiliary Storage for the Computer.

Convenient handling of asynchronous data such as is described in sections 4.1 and 4.2 cannot be done without the use of dual heads. Since only 12 of these heads will be supplied and these must be used in pairs, it is apparent that a few groups on the buffer drum will be available for use in a manner identical with those on the auxiliary drum. Such a provision may offer advantages to a programmer other than a simple extension of the auxiliary storage capacity. Some points for consideration are the following.

(1) The heads in the buffer drum have electronic switching of their writing circuits so new groups can be selected without the 24 millisecond wait required in the auxiliary drum.

(2) With physically separate drums, one can have two drum groups to refer to without the necessity for switching groups.

(3) If it is desired to refer to single registers in succession so that drum addresses would not have to be specified, one can have two fields for this, either for reading, for recording, or for reading and recording.

SIGNED E S Rich
E. S. Rich

Drawing Attached No. SA-50699
ESR/cp

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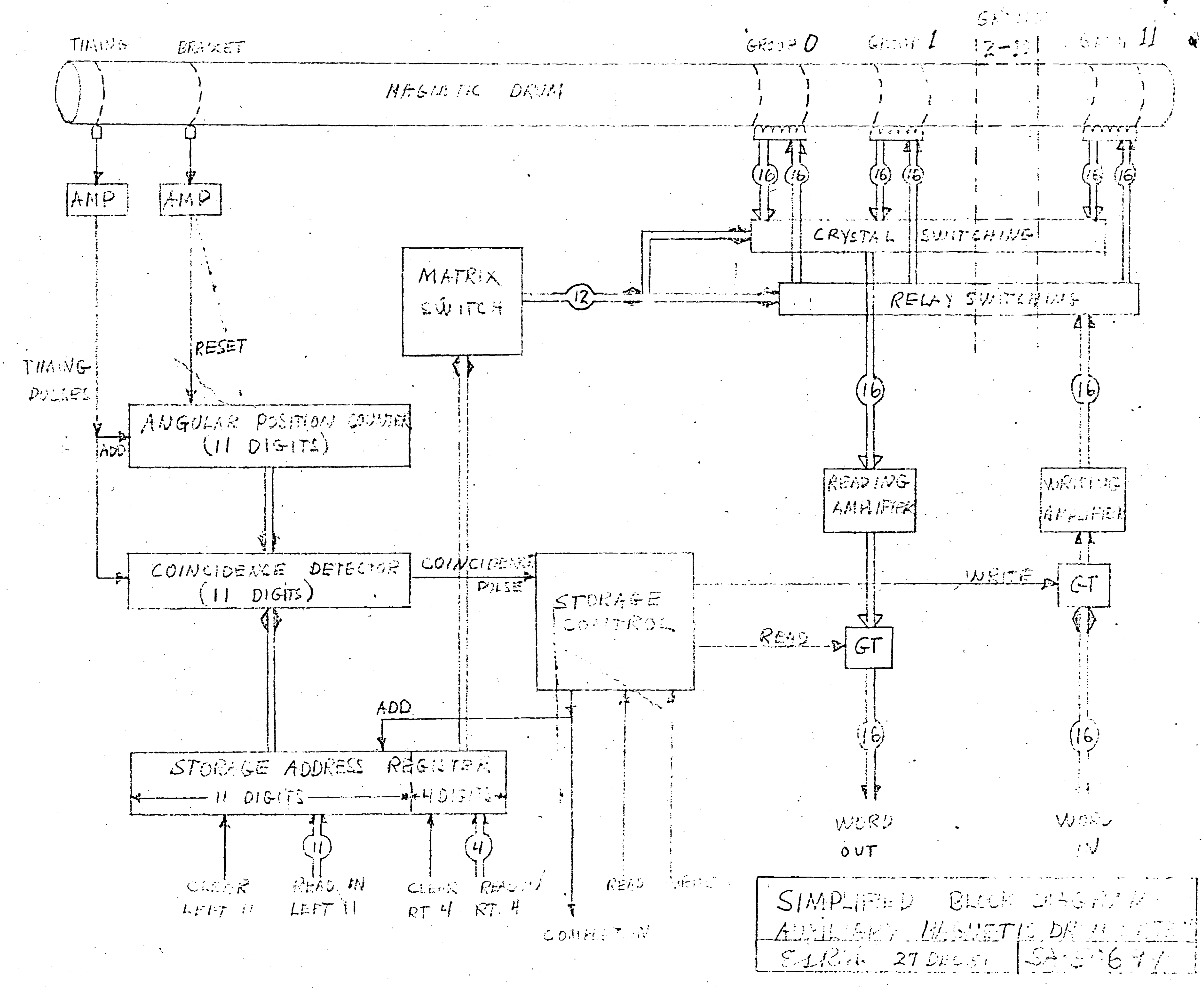
H. Fahnestock
N. H. Taylor
J. A. O'Brien
C. R. Wieser
S. H. Dodd
C. W. Adams
R. L. Walquist
L. R. Brown
B. E. Morriss
P. W. Stephan
J. T. Gilmore
J. H. Hughes
L. R. Israel
R. P. Mayer
C. W. Watt
J. A. Arnow
J. W. Carr
N. L. Leggett


TIMING
BRACKET
MAGNETIC DRUM
GROUP 0
GROUP 1
GROUP 11
16
AMP
AMP
CRYSTAL SWITCHING
MATRIX SWITCH
12
RELAY SWITCHING
RESET
TIMING PULSES
ANGULAR POSITION COUNTER (11 DIGITS)
ADD
READING AMPLIFIER
WRITING AMPLIFIER
COINCIDENCE DETECTOR (11 DIGITS)
COINCIDENCE PULSE
STORAGE CONTROL
WRITE
GT
READ
ADD
STORAGE ADDRESS REGISTER
11 DIGITS
4 DIGITS
11
4
CLEAR LEFT 11
READ IN LEFT 11
CLEAR RT 4
READ IN RT. 4
READ
WORD OUT
WORD IN
SIMPLIFIED BLOCK DIAGRAM
AUXILIARY MAGNETIC DRUM UNIT